LATCH-BASED PULSE GENERATOR

Abstract of the Disclosure

There is provided a pulse generator capable of generating a pulse with a reduced number of transistors that toggle in response to a clock signal, thereby reducing power consumption. The pulse generator includes a plurality of unit cells, wherein an n^{th} unit cell (n is a natural number more than 2) generates a pulse in response to a divided-by-N clock signal (N is a natural number), a signal output from an $(n-1)^{th}$ unit cell and a signal output from an $(n+1)^{th}$ unit cell. The n^{th} unit cell is reset or generates the pulse whose width is equivalent to the width of the clock signal, according to the logic level of the signal output from the $n+1^{th}$ unit cell.